Silicon NPN Power Transistors 2SD1554

DESCRIPTION

·With TO-3P(H)IS package
·Built-in damper diode
·High voltage ,high speed
·Low collector saturation voltage

APPLICATIONS

·For color TV horizontal output applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

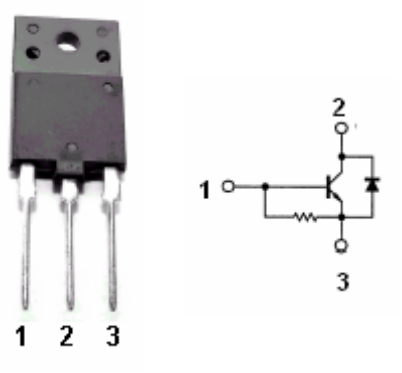

Fig.1 simplified outline (TO-3P(H)IS) and symbol

Absolute maximum ratings (Ta=25□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	1500	V
V_{CEO}	Collector-emitter voltage	Open base	600	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		3.5	A
I_B	Base current		1	A
P_C	Collector power dissipation	T_C=25□	40	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E=0.2A , I_C=0	5			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=3A; I_B=0.8A		5.0	8.0	V
V_{BEsat}	Base-emitter saturation voltage	I_C=3A ;I_B=0.8A			1.5	V
I_{CBO}	Collector cut-off current	V_{CB}=500V; I_E=0			10	μA
h_{FE}	DC current gain	I_C=0.5A ; V_{CE}=5V	8			
f_T	Transition frequency	I_C=0.1A ; V_{CE}=10V		3		MHz
C_{OB}	Collector output capacitance	I_E=0 ; V_{CB}=10V;f=1MHz		95		pF
V_F	Diode forward voltage	I_F=3.5A			2.0	V
t_f	Fall time	I_{CP}=3A ;$I_{B1(end)}$=0.8A		0.5	1.0	μs

PACKAGE OUTLINE

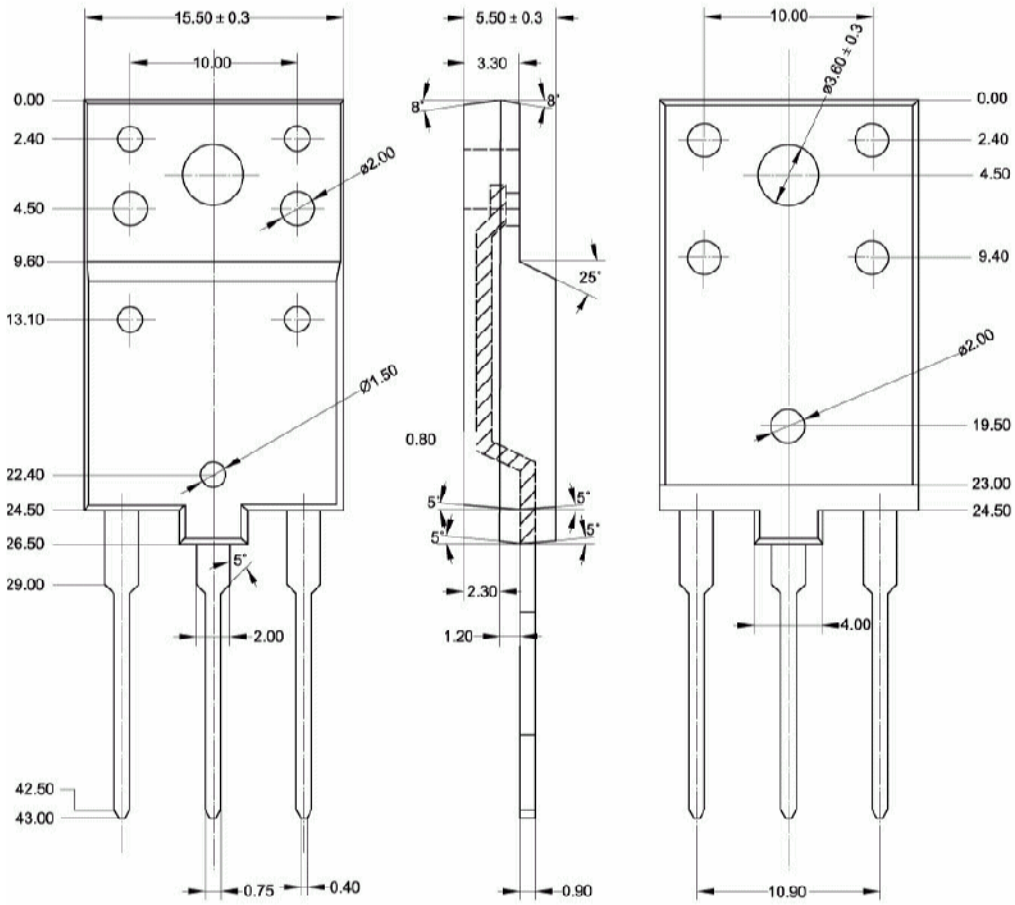

Fig.2 Outline dimensions (unindicated tolerance:±0.15 mm)